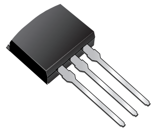
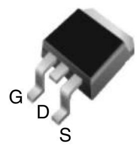
Power MOSFET

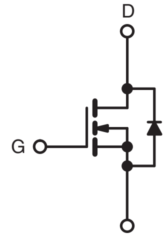
PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 5 V	0.05
Q_g (Max.) (nC)	35	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	25	
Configuration	Single	

I^2PAK (TO-262)



D^2PAK (TO-263)





N-Channel MOSFET

FEATURES

- Advanced Process Technology
- Surface Mount (IRLZ34S/SiHLZ34S)
- Low-Profile Through-Hole (IRLZ34L/SiHLZ34L)
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast swichting speed and ruggedized device design that Power MOSFETs are known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.
The D^2PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRLZ34L/SiHLZ34L) is available for low-profile applications.

ORDERING INFORMATION		
Package	D^2PAK (TO-263)	I^2PAK (TO-262)
SnPb	IRLZ34S	IRLZ34L
	SiHLZ34S	SiHLZ34L

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

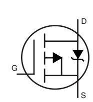
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5 V	T_C = 25 °C	I_D	30	A
		T_C = 100 °C		21	
Pulsed Drain Current[a]			I_{DM}	110	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	220	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	88	W
Maximum Power Dissipation (PCB Mount)[e]	T_A = 25 °C			3.7	
Peak Diode Recovery dV/dt[c]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, Starting T_J = 25 °C, L = 290 µH, R_G = 25 Ω, I_{AS} = 30 A (see fig. 12).
c. $I_{SD} \leq 30$ A, dI/dt ≤ 200 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	1.7	

Note
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.07	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 5 V	I_D = 18 A[b]	-	-	0.05	Ω
		V_{GS} = 4 V	I_D = 15 A[b]	-	-	0.07	
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 18 A		12	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1600	-	pF
Output Capacitance	C_{oss}			-	660	-	
Reverse Transfer Capacitance	C_{rss}			-	170	-	
Total Gate Charge	Q_g	V_{GS} = 5 V	I_D = 30 A, V_{DS} = 48 V, see fig. 6 and 13[b]	-	-	35	nC
Gate-Source Charge	Q_{gs}			-	-	7.1	
Gate-Drain Charge	Q_{gd}			-	-	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 30 A, R_G = 6 Ω, R_D = 1 Ω, see fig. 10[b]		-	14	-	ns
Rise Time	t_r			-	170	-	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	t_f			-	56	-	
Internal Source Inductance	L_S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	30	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	110	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 30 A, V_{GS} = 0 V[b]		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 30 A, dI/dt = 100 A/µs[b]		-	120	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	700	1300	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

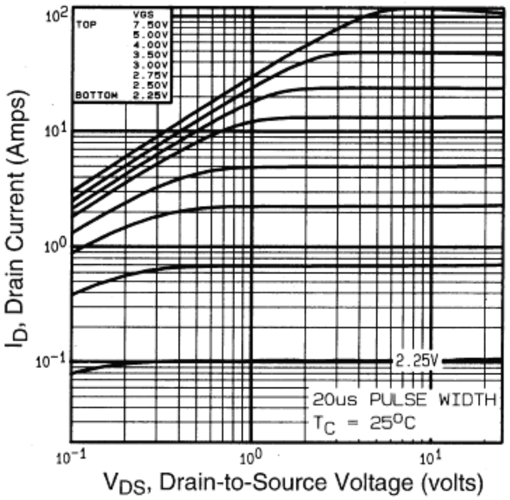

Fig. 1 - Typical Output Characteristics, T_C = 25 °C

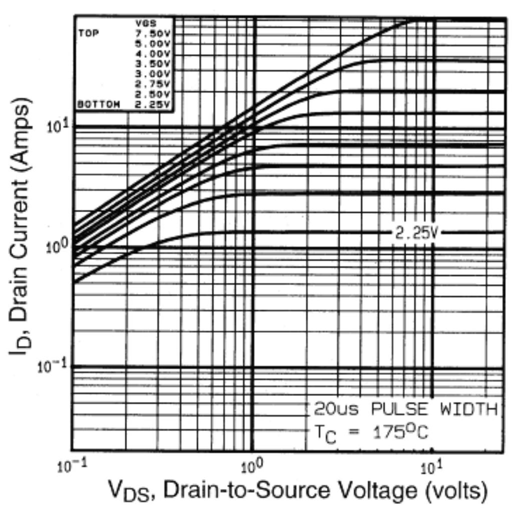

Fig. 2 - Typical Output Characteristics, T_C = 175 °C

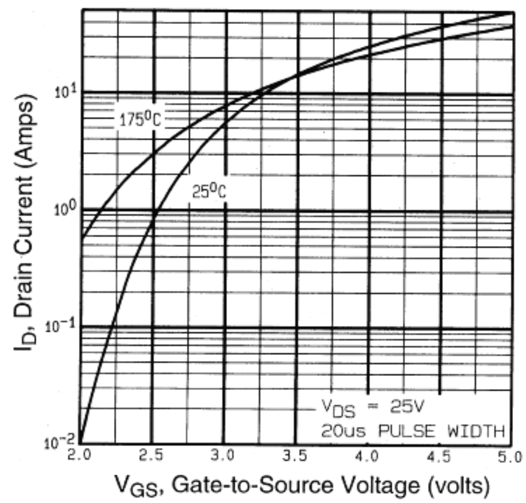

Fig. 3 - Typical Transfer Characteristics

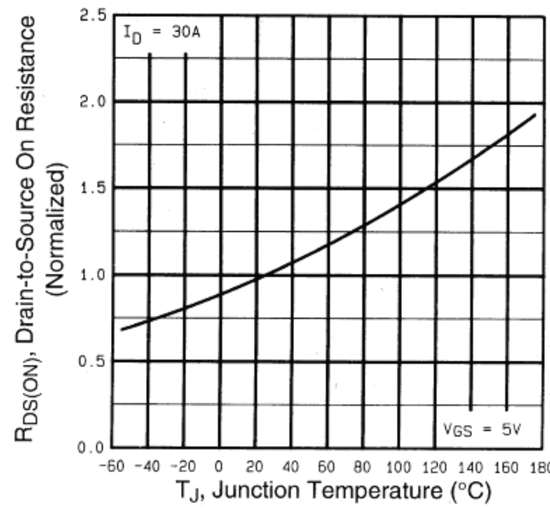

Fig. 4 - Normalized On-Resistance vs. Temperature

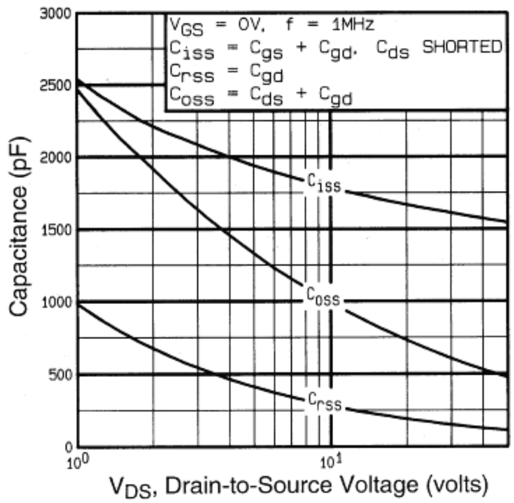

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

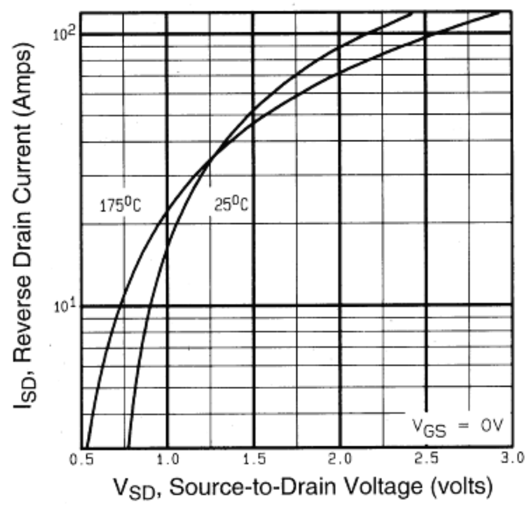

Fig. 7 - Typical Source-Drain Diode Forward Voltage

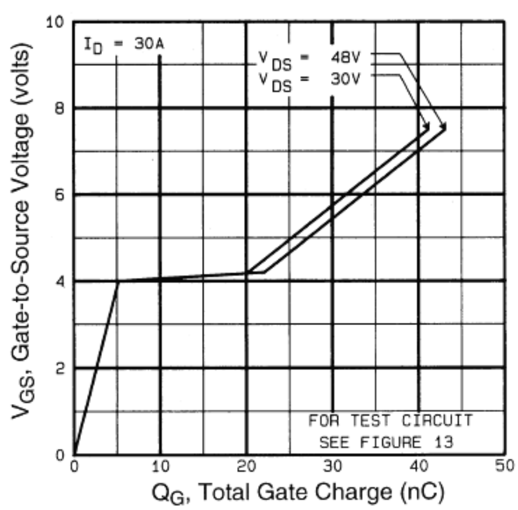

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

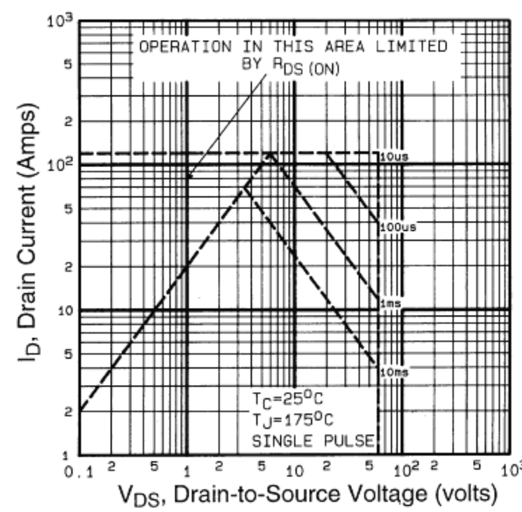

Fig. 8 - Maximum Safe Operating Area

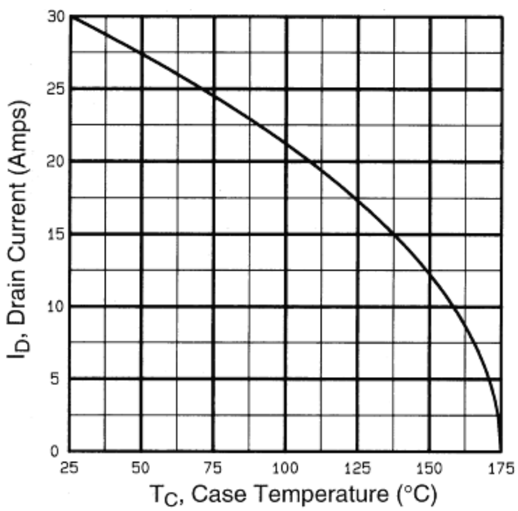

Fig. 9 - Maximum Drain Current vs. Case Temperature

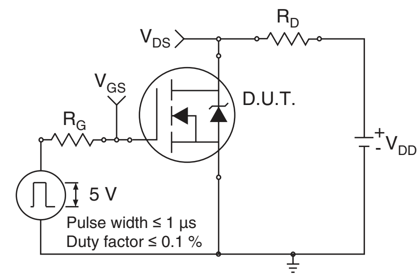

Fig. 10a - Switching Time Test Circuit

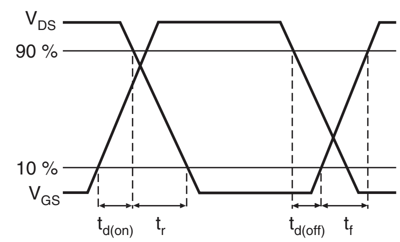

Fig. 10b - Switching Time Waveforms

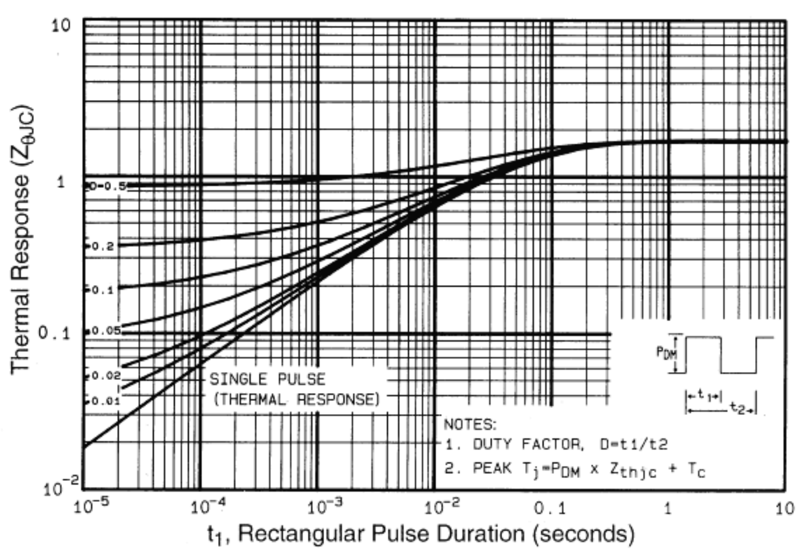

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

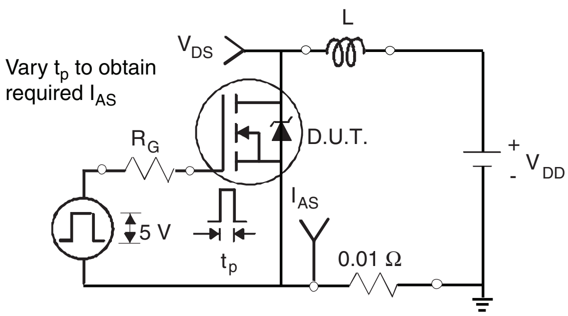

Fig. 12a - Unclamped Inductive Test Circuit

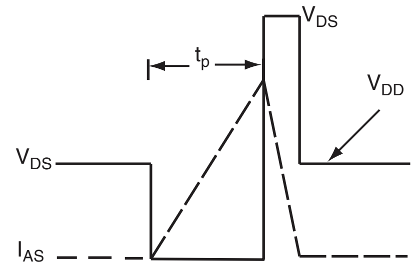

Fig. 12b - Unclamped Inductive Waveforms

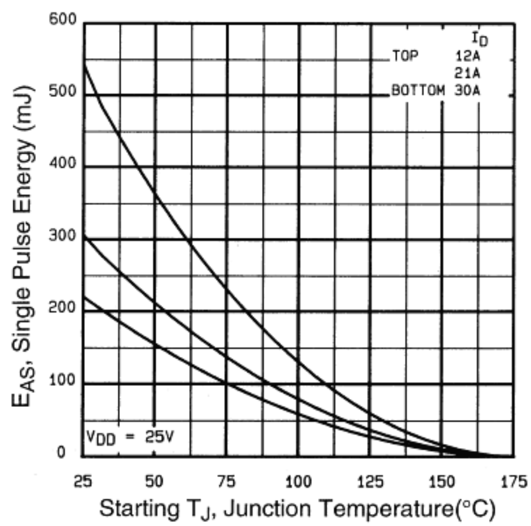

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

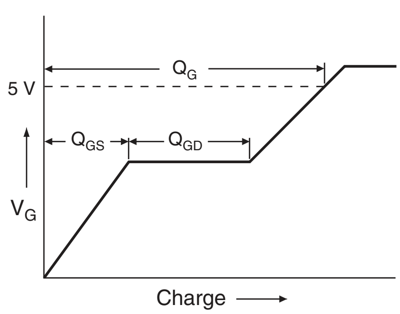

Fig. 13a - Basic Gate Charge Waveform

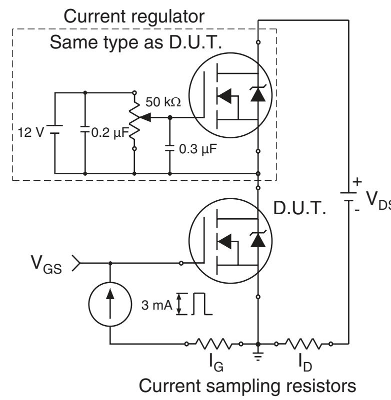

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

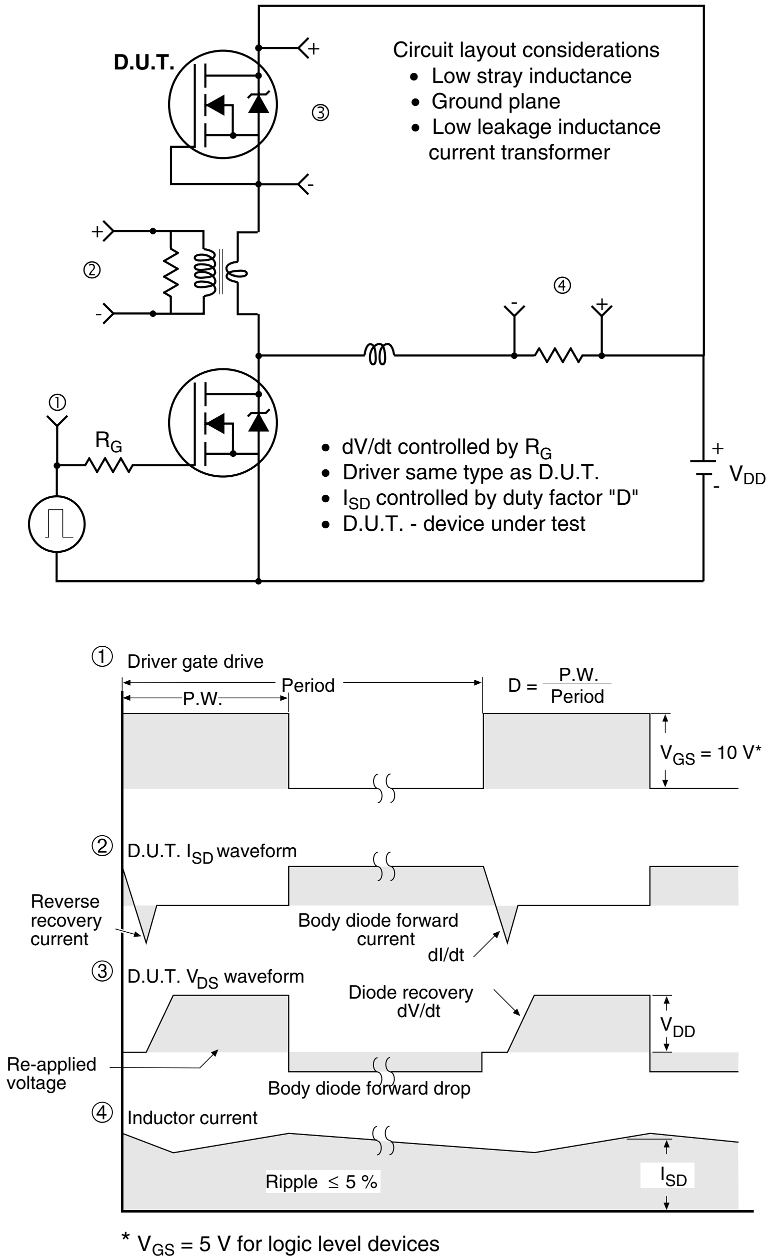

Fig. 14 - For N-Channel

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